What is claimed is:

1. A method of designing digital signal processing hardware to implement a z-domain transfer function, wherein the processing of signal samples is characterized by constant latency, the method comprising:
    a) specifying said transfer function;
    b) without regard to latency characteristics, specifying a first hardware stage to process said signal samples in accordance with said transfer function; and
    c) specifying a second hardware stage to dynamically selectively delay said signal samples processed by said first hardware stage such that the combined first and second stage latency for the processing of said signal samples is a constant.

2. The method of designing digital signal processing hardware of claim 1, wherein said first hardware stage is a generic data processor.

3. The method of designing digital signal processing hardware of claim 1, wherein said second hardware stage includes a multistage FIFO.

4. The method of designing digital signal processing hardware of claim 1, wherein said second stage includes a selector that couples to the second stage output a selected one of a plurality of sequentially delayed variations of the samples provided to the second stage input.

5. The method of designing digital signal processing hardware of claim 4, wherein the selector control is a function of shifts into and out of said first stage.

6. The method of designing digital signal processing hardware of claim 4, wherein the selector control includes an up/down counter.

7. The method of designing digital signal processing hardware of claim 1, further including:

independent of said specifying of said first hardware stage, specifying the target implementation technology.

8. The method of designing digital signal processing hardware of claim 7, wherein the target implementation technology is a design approach selected from the group consisting of FPGA, ASIC, semi-custom, and custom.

9. The method of designing digital signal processing hardware of claim1, further including:

independent of said specifying of said first hardware stage, specifying the target arithmetic library.

10. The method of designing digital signal processing hardware of claim 1, further including:

a) specifying a first technology as the target implementation technology; and

b) after said specifying of said target implementation technology and said specifying of said first hardware stage, and without requiring modification of the specification of said first hardware stage, changing the target implementation technology to a second technology.

11. The method of designing digital signal processing hardware of claim 1, further including:

a) specifying a test bench for the testing of the transfer function, said test bench including simulation modules and test vectors, said transfer function being conceptually modeled as being of the form $z^{-N} \times T(z)$, where $T(z)$ is the desired transfer function and where the realization of the z^{-N} delay may be configured independent of other aspects of the test bench;

b) specifying a first technology as the target implementation technology and specifying the z^{-N} delay based on the target implementation technology;

c) after said specifying of said first hardware stage, said test bench, said target implementation technology, and said z^{-N} delay, changing the target implementation technology to a second technology without requiring revised specification of said first hardware stage and without requiring modification of said test bench beyond the revised specification of said z^{-N} delay in accordance with the second technology.

12. The method of designing digital signal processing hardware of claim 1, further including:

a) specifying a first library as the target arithmetic library; and

b) after said specifying of said first library and said specifying of said first hardware stage, and without requiring modification of the specification of said first hardware stage, changing the target arithmetic library to a second library.

13. The method of designing digital signal processing hardware of claim 1, further including:

a) specifying a test bench for the testing of the transfer function, said test bench including simulation modules and test vectors, said transfer function being conceptually modeled as being of the form $z^{-N} \times T(z)$, where T(z) is the desired transfer function and where the realization of the z^{-N} delay may be configured independent of other aspects of the test bench;

b) specifying a first library as the target arithmetic library and specifying the z^{-N} delay based on the target arithmetic library;

c) after said specifying of said first hardware stage, said test bench, said target arithmetic library, and said z^{-N} delay, changing the target arithmetic library to a second library without requiring revised specification of said first hardware stage and without requiring modification of said test bench beyond the revised specification of said z^{-N} delay in accordance with the second library.

14. A method of operating digital signal processing hardware to implement a z-domain transfer function, wherein the processing of signal samples is characterized by constant latency, the method comprising:

a) providing a first and second hardware stage;

b) configuring and operating said first hardware stage to process said signal samples in accordance with said transfer function, said first hardware stage processing said signal samples with variable latency; and

c) operating said second hardware stage to dynamically selectively delay said signal samples processed by said first hardware stage such that the combined first and second stage latency for the processing of said signal samples is a constant.

15. The method of operating digital signal processing hardware of claim 14, wherein said first hardware stage is a generic data processor.

16. The method of operating digital signal processing hardware of claim 14, wherein said second hardware stage includes a multistage FIFO.

17. The method of operating digital signal processing hardware of claim 14, wherein said second stage includes a selector that couples to the second stage output a selected one of a plurality of sequentially delayed variations of the samples provided to the second stage input.

18. The method of operating digital signal processing hardware of claim 17, wherein the selector control is a function of shifts into and out of said first stage.

19. The method of operating digital signal processing hardware of claim 17, wherein the selector control includes an up/down counter.

20. Circuitry for implementing a z-domain transfer function for the processing of signal samples, the circuitry comprising:

a) transfer function circuitry, said transfer function circuitry processing said signal samples in a first variable length pipeline in accordance with said transfer function, said transfer function circuitry processing V samples at any given time;

b) delay circuitry following said transfer function circuitry, said delay circuitry delaying in a second variable length pipeline signal samples processed previously by said transfer function circuitry, said delay circuitry delaying D of samples at any given time; and

c) delay circuitry control logic coupled to said transfer function circuitry and said delay circuitry and dynamically adjusting the number of said D samples to maintain the sum of V and D as a constant.

21. The circuitry for implementing a z-domain transfer-function of claim 20, wherein said transfer function circuitry includes a generic data processor.

22. The circuitry for implementing a z-domain transfer function of claim 20, wherein said second delay circuitry includes a multistage FIFO.

23. The circuitry for implementing a z-domain transfer function of claim 20, wherein said delay circuitry includes a selector that couples to the delay circuitry output a selected one of a plurality of sequentially delayed variations of the samples provided to the delay circuitry input.

24. The circuitry for implementing a z-domain transfer function of claim 23, wherein the delay circuitry control is a function of shifts into and out of said transfer function circuitry.

25. The circuitry for implementing a z-domain transfer function of claim 23, wherein the delay circuitry control includes an up/down counter.

26. A digital signal processing building bock for processing block-input signal samples to create block-output signal samples in accordance with the closed-loop z-domain transfer function A(z)/(1+A(z), where A(z) is an open-loop transfer function, the building block comprising:

a) B(z) transfer function circuitry having a B(z)-input and a B(z)-output, said B(z) transfer function circuitry processing signal samples received at the B(z)-input in a first variable length pipeline in accordance with a B(z) transfer function, said B(z) transfer function circuitry processing V signal samples at any given time;

b) D(z) delay circuitry following said B(z) transfer function circuitry, wherein $A(z) = B(z) \times D(z)$, said D(z) delay circuitry delaying in a second variable length pipeline samples received from said B(z)-output, the delay circuitry delaying D signal samples at any given time before providing them as the block-output signal samples;

c) D(z) delay circuitry control logic coupled to said B(z) transfer function circuitry and said D(z) delay circuitry and dynamically adjusting the pipeline length of D(z) to maintain the sum of V and D as a constant;

d) a summer having a positive input, a negative input, and a difference output, said positive input receiving block-input signal samples, said negative input receiving said block-output signal samples, said difference output providing difference signal samples to the B(z)-input.

27. The digital signal processing building bock of claim 26, wherein said B(z) transfer function circuitry includes a generic data processor.

28. The digital signal processing building bock of claim 26, wherein said D(z) delay circuitry includes a multistage FIFO.

29. The digital signal processing building bock of claim 26, wherein said D(z) delay circuitry includes a selector that couples to the block-output a selected one of a plurality of sequentially delayed variations of the samples provided by the B(z)-output.

30. The digital signal processing building bock of claim 26, wherein the D(z) delay circuitry control is a function of shifts into and out of said B(z) transfer function circuitry.

31. The digital signal processing building bock of claim 26, wherein the D(z) delay circuitry control includes an up/down counter.